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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,122	08/25/2003	T. Warren Weeks	N0400.70017US00	5512

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/650,122	WEEKS ET AL.
	Examiner	Art Unit
	Eugene Lee	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *40-42,44,45,47-49 and 106-145* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *40-42,44,45,47-49 and 106-145* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the electrically conductive material is in direct contact with the first electrical contact (claim 126), the first electrical contact being formed, in part, from the electrically conductive material formed in the via (claim 127), the first electrical contact extends to a backside of the semiconductor device (claim 128), the first electrical contact extends from a topside of the semiconductor device to the backside of the semiconductor device (claim 129), the first electrical contact is formed, in part, on the backside of the semiconductor device (claim 130), and the via extends from a topside of the semiconductor device (claim 134) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 126 thru 143 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not describe the electrically conductive material being in direct contact with the first electrical contact (claim 126), the first electrical contact being formed, in part, from the electrically conductive material formed in the via (claim 127), the first electrical contact extends to a backside of the semiconductor device (claim 128), the first electrical contact extends from a topside of the semiconductor device to the backside of the semiconductor device (claim 129), the first electrical contact is formed, in part, on the backside of the semiconductor device (claim 130), and the via extends from a topside of the semiconductor device (claim 134).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 40 thru 42, 47 thru 49, 106 thru 112, 115, 116, 123 thru 125, 127, 144, and 145 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenz et al. 4,537,654 in view of Takayama et al. 6,521,917 B1. Berenz discloses (see, for example, FIG. 1) a field-effect transistor (semiconductor device) comprising a substrate 16, active layer (material region) 10, drain contact (first electrical contact) 18, gate element (second electrical contact) 12, and metallized via hole (via and having electrically conductive material formed therein) 19. Berenz does not disclose the material region being gallium nitride. However, Takayama discloses (see, for example, column 10, line 62-column 11, line 10) transistors comprising semiconductor structures such as GaN (gallium nitride). Takayama further states that GaN has wide band gap, high breakdown electronic field, and high saturation velocity. Therefore, it would have been obvious to one of ordinary skill in the art to have the material region being gallium nitride in order to have wide band gap, high breakdown electronic field, and high saturation velocity.

Regarding claim 41, see, for example, FIG. 1 wherein Berenz discloses the left portion of drain contact (first electrical contact) 18 on a sloped plane of active layer 10, and gate element (second electrical contact) 12 on a horizontal plane of active layer 10.

Regarding claim 42, see, for example, FIG. 1 wherein Berenz discloses the right portion of drain contact (first electrical contact) 18, and gate element (second electrical contact) 12 on the same horizontal plane of active layer 10.

Regarding claims 47-49, and 107, and the limitations "the semiconductor device is a light emitting device" (claim 47), "an LED" (claim 48), "a light-detecting device" (claim 49), and "the first electrical contact is a source electrode, the second electrical contact is a drain electrode, and the third electrical contact is a gate electrode" (claim 107), it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPZ F. 2d 1647 (1987).

Regarding claim 106, see, for example. FIG. 1 wherein Berenz discloses another gate element (third electrical contact) 112.

Regarding claims 109-111, see, for example, column 5, lines 3-9 wherein Berenz discloses the metal layer of titanium (second material) and gold (first material). It would have been obvious to one of ordinary skill in the art at the time of invention to have this metal layer in order to have a contact of adequate conductivity.

Regarding claim 115, see, for example, FIG. 1 wherein Berenz discloses the via extending to source region at 14.

6. Claims 44, 45, and 113 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenz et al. '654 in view of Takayama et al. '917 B1 as applied to claims 40-42, 47-49, 106-112, 115, 116, 123-125, 127, 144, and 145 above, and further in view of Edmond et al.

6,120,600. Berenz in view of Takayama does not disclose a transition layer. However, Edmond discloses (see, for example, FIG. 2) a semiconductor device comprising a buffer layer (transition layer) 42. The buffer layer comprises an $Al_xGa_{1-x}N$ layer (compositionally-graded, claim 45) and an AlN layer (constant transition layer). In column 7, lines 39-40, Edmond discloses the buffer layer as insulating rather than conductive. It would have been obvious to one of ordinary skill in the art at the time of invention to have a transition layer in order to insulate the substrate from the active layer and minimize lattice mismatching between layers.

7. Claim 114 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berenz et al. '654 in view of Takayama et al. '917 B1 as applied to claims 40-42, 47-49, 106-112, 115, 116, 123-125, 127, 144, and 145 above, and further in view of Khan et al. 5,192,987. Berenz in view of Takayama does not disclose an AlGaN layer. However, Khan discloses (see, for example, FIG. 4) a semiconductor device comprising an $Al_xGa_{1-x}N$ layer (AlGaN layer) 41. In column 4, lines 27-34, Khan discloses that the electron gas mobilities will be several times greater than the bulk material electrons. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an AlGaN layer in order to increase the electron mobilities.

8. Claims 117, 121, and 122 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenz et al. '654 in view of Takayama et al. '917 B1 as applied to claims 40-42, 47-49, 106-112, 115, 116, 123-125, 127, 144, and 145 above, and further in view of Vaudo et al. 6,156,581. Berenz in view of Takayama does not disclose a substrate made of silicon, sapphire, or silicon carbide. However, Vaudo discloses (see, for example, column 1, lines 32-49) GaN-based

devices having sapphire, silicon carbide, and silicon substrates. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a silicon, sapphire, or silicon carbide substrate in order to have a base to form a GaN layer for a semiconductor device.

9. Claims 118 thru 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenz et al. '654 in view of Takayama et al. '917 B1 in view of Vaudo et al. '581 as applied to claims 117, 121, and 122 above, and further in view of Edmond et al. 6,120,600. Berenz in view of Takayama in view of Vaudo does not disclose a gallium nitride alloy between the silicon substrate and the gallium nitride material layer, wherein a gallium concentration in the transition layer is increased from a back surface of the transition layer to a top surface of the transition layer. However, Edmond discloses (see, for example, FIG. 2) a semiconductor device comprising a buffer layer (transition layer) 42. The buffer layer comprises an $Al_xGa_{1-x}N$ layer (gallium nitride alloy). In column 7, lines 18-24, Edmond discloses the buffer layer is progressive graded with increasing amounts of gallium until it is substantially entirely gallium nitride at its upper surface. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a gallium nitride alloy between the silicon substrate and the gallium nitride material layer, wherein a gallium concentration in the transition layer is increased from a back surface of the transition layer to a top surface of the transition layer in order to insulate the substrate from the active layer and minimize lattice mismatching between layers.

Regarding claims 119, and 120, Berenz in view of Takayama in view of Vaudo in view of Edmond does not disclose the gallium nitride material region having a thickness of greater than 0.5 micron or 1.0 micron, and a crack level of less than 0.005 micron/micron^2. However, it

was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the thickness of a gallium nitride material and the crack level in order to provide an active layer that has a low resistance for transmitting a current. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the gallium nitride material region having a thickness of greater than 0.5 micron and a crack level of less than 0.005 micron/micron^2 because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the thickness of the gallium nitride material and the crack level in order to provide an active layer that has a low resistance for transmitting a current. See In re Aller, 105 USPQ 233.

Response to Arguments

10. Applicant's arguments with respect to claims 40-42, 44, 45, 47-49, and 106-145 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
August 23, 2005